UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,822	04/09/2004	Stephen H. Gunther	42P4728XC	1387

8791 7590 12/05/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/821,822	GUNTHER ET AL.	
	Examiner	Art Unit	
	Tung S. Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37,44,45,52,53 and 60* is/are rejected.

7)☒ Claim(s) *38-43,46-51 and 54-59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *see office action*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Preliminary Amendment

1. Preliminary Amendment filed on 04/09/2004 is noted by the examiner.

Information Disclosure Statement

2. The information disclose statement filed 04/09/2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. Item 48-53 is missing from the application file. Applicant is required to submit a legible copy of 48-53. The parent application (09/784255) does not contain such documents.

Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purpose of determining compliance with the requirements based on the time of filling the statement, including all certification requirements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).
A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).
Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 37, 45 and 53 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 8, and 15 of U.S. Patent No. 6,789,037. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations of the claims in the current application are encompassed in the U.S. Patent No. 6,789,037.

The current pending application encompasses the same process as the pending application and is a slightly broader version of the U.S. Patent No. 6,789,037.

(Underlined portions below, show the differences in the process)

Claim 1 (10/821822)	Claim 8 (U.S. Patent No. 6,789,037)
37. A thermal management system for an integrated circuit die comprising: a temperature sensor formed directly on the die, the temperature sensor having an output; a power modulation element formed directly on the die, the power modulation element to reduce power consumption of the die in response to the output of the temperature sensor; a control element formed directly on the die, the control element including at least one register to provide an enable/disable bit for the thermal management system; and	8. A microprocessor comprising: a die having a plurality of functional units formed thereon; internal clock circuitry formed on the die and coupled to at least one of the plurality of functional units; and a thermal management system formed directly on the die, the thermal management system including a temperature detection element including at least one temperature sensor having an output, the at least one temperature sensor including a reference voltage source providing a reference voltage, a programmable voltage source providing a programmable voltage proportional to a temperature of the die, and a comparator having one input coupled via a first signal line to the

a visibility element formed directly on the die, the visibility element to indicate a status of the output of the temperature sensor. .	reference voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the at least one temperature sensor in response to the programmable voltage substantially equaling the reference voltage; a power modulation element to reduce power consumption of at least one of the functional units in response to the output of the at least one temperature sensor; a control element including at least one register to provide an enable/disable bit for the thermal management system; and a visibility element to indicate a status of the output of the at least one temperature sensor.
Claim 45 (10/821822)	Claim 8 (U.S. Patent No. 6,789,037)
45. An apparatus comprising: a die; and a thermal management system formed directly on the die, the thermal management system including a temperature sensor, the temperature sensor having an output; a power modulation element to reduce power consumption of the die in response to the output of the temperature sensor, a control element including at least one register to provide an enable/disable bit for the thermal management system; and	8. A microprocessor comprising: a die having a plurality of functional units formed thereon; internal clock circuitry formed on the die and coupled to at least one of the plurality of functional units; and a thermal management system formed directly on the die, the thermal management system including a temperature detection element including at least one temperature sensor having an output, the at least one temperature sensor including a reference voltage source providing a reference voltage, a programmable voltage source providing a programmable voltage

a visibility element to indicate a status of the output of the temperature	proportional to a temperature of the die, and a comparator having one input coupled via a first signal line to the reference voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the at least one temperature sensor in response to the programmable voltage substantially equaling the reference voltage; a power modulation element to reduce power consumption of at least one of the functional units in response to the output of the at least one temperature sensor; a control element including at least one register to provide an enable/disable bit for the thermal management system; and a visibility element to indicate a status of the output of the at least one temperature sensor.
Claim 53 (10/821822)	Claim 15 (U.S. Patent No. 6,789,037)
53, A system comprising: a memory coupled with a bus; and a processor coupled with the bus, the processor including a die and a thermal management system formed directly on the die, the thermal management system including a temperature sensor, the temperature sensor having an output; a power modulation element, the power	15. A computer system comprising: at least one memory device coupled to a bus; and at least one microprocessor coupled to the bus, the at least one microprocessor including a die having a plurality of functional units formed thereon; internal clock circuitry formed on the die and coupled to at least one of the plurality of functional units; and a thermal management system located on the die, the thermal

modulation element to reduce power consumption of the processor in response to the output of the temperature sensor; a control element, the control element including at least one register to provide an enable/disable bit; and a visibility element, the visibility element to indicate a status of the output of the temperature sensor.	management system including a temperature detection element formed directly on the die, the temperature detection element including at least one temperature sensor having an output, the at least one temperature sensor including a reference voltage source providing a reference voltage, a programmable voltage source providing a programmable voltage proportional to a temperature of the die, and a comparator having one input coupled via a first signal line to the reference voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the at least one temperature sensor in response to the programmable voltage substantially equaling the reference voltage; a power modulation element formed directly on the die, the power modulation element to reduce power consumption of at least one of the functional units in response to the output of the at least one temperature sensor; a control element formed directly on the die, the control element including at least one register to provide an enable/disable bit; and a visibility element formed directly on the die, the visibility element to indicate a status of the output of the at least one temperature sensor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

a. Claims 37, 44, 45, 52, 53 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussain et al. (U.S. Patent 6,172,611) in view of Gose et al. (U.S. Patent 5,675,297).

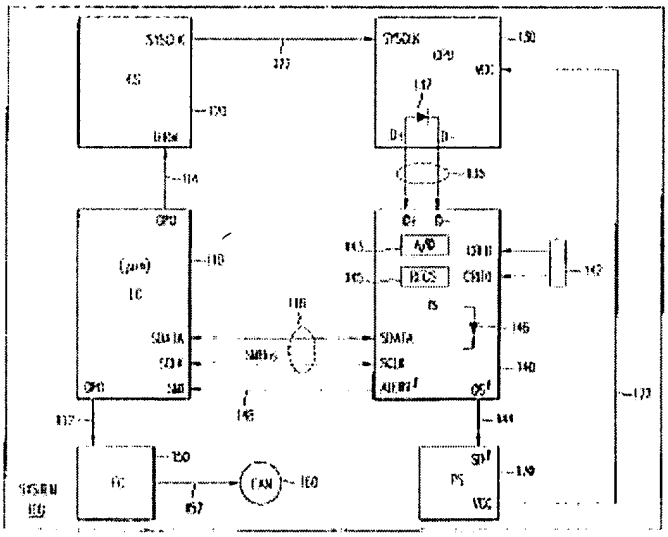
Regarding claim 37:

Hussain discloses a thermal management system for an integrated circuit die comprising: a temperature sensor formed directly on the die (Col. 2, Lines 40-60), the temperature sensor having an output (fig. 3, unit 340, 350); the element to reduce power consumption of the die in response to the output of the temperature sensor (fig. 1, unit 130); a control element formed directly on the die (fig. 1, unit 120), the control element including at least one register to provide an enable/disable bit for the thermal management system; and a visibility element formed directly on the die (fig. 2, unit 20), the visibility element to indicate a status of the output of the temperature sensor (fig. 3, unit 360, 350).

Regarding claim 45:

Hussain discloses an apparatus comprising: a die; and a thermal management system formed directly on the die (Col. 2, Lines 40-60), the thermal management system including a temperature sensor (fig. 3, unit 340, 350), the temperature

sensor having an output (fig. 3, unit 340, 350); a element to reduce power consumption of the die in response to the output of the temperature sensor, (Col. 2, Lines 40-60) a control element including at least one register to provide an enable/disable bit for the thermal management system (fig. 2, unit 230, 240); and a visibility element to indicate a status of the output of the temperature (fig. 3, unit 365).



FIC. 1

Regarding claim 53:

Hussain discloses a system comprising: a memory coupled with a bus (fig. 2, unit 210); and a processor coupled with the bus (fig. 1, unit 130), the processor including a die and a thermal management system formed directly on the die (fig. 1, unit 143, 145), the thermal management system including a temperature sensor (fig. 1, unit 150, 140), the temperature sensor having an output (fig. 1, unit 152); the element to reduce power consumption of the processor in response to the output of the temperature sensor (Col. 3-4, Lines 40-28); a control element,

the control element including at least one register to provide an enable/disable bit; and a visibility element (fig. 2, unit 230, 240), the visibility element to indicate a status of the output of the temperature sensor (fig. 2, unit 240), 230).

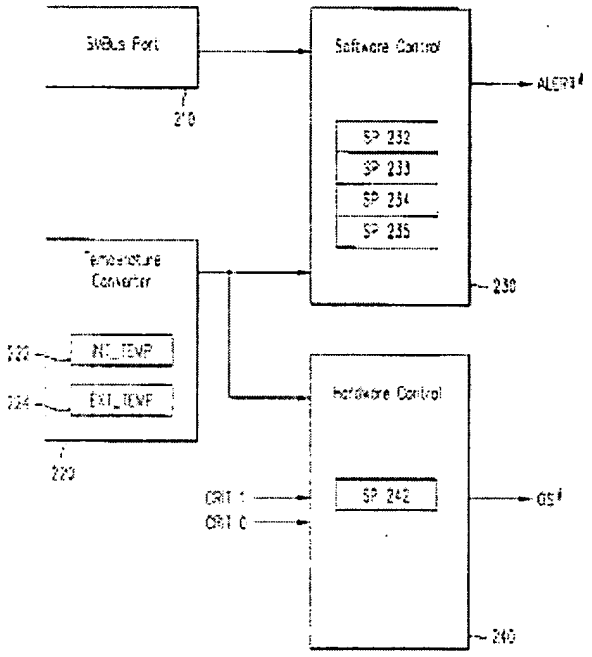


FIG. 2

Regarding claims 44, 52 and 60, Hussain discloses lower a frequency of a clock signal internal to the die (Col. 3, Lines 47-67).

Hussain does not disclose power modulation, Gose disclose power modulation (Col. 2, Lines 5-30), in order to provide a short circuit protection and thermo protection of the circuit to avoid permanent damage (Col. 2, Lines 41-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hussain to have power modulation taught by Gose

in order to provide a short circuit protection and thermo protection of the circuit to avoid permanent damage (Col. 2, Lines 41-47).

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. I , 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Hussain and Gose are analogous art because they are from the same field of endeavor, thermal control in a integrated circuit.

Allowable Subject Matter

5. Claims 38-43, 46-51 and 54-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitation of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: prior art fail to teach regarding claims 38, 46 and 54, a programmable voltage source providing a programmable voltage proportional to a temperature of the die; and a comparator having one input coupled via a first signal line to the reference

voltage source and another input coupled via a second signal line to the programmable voltage source, the comparator to provide a signal at the output of the temperature sensor in response to the programmable voltage substantially equaling the reference voltage; regarding claims 42, 50 and 58, including at least one of a register to selectively disengage a specified portion of the thermal management system, a register to enable the thermal management system in response to an occurrence of an external event, a register to force the thermal management system active while overriding a disable bit provided by the at least one register, and a register to allow external software and hardware to enable the thermal management system; regarding claims 43, 51 and 59, a register to provide a sticky bit, a counter to count a number of lost clock cycles resulting from operation of the thermal management system, and circuitry to generate an interrupt when the temperature sensor output transitions to a different state.

Claims 39-41 are objected due to their dependency on claim 38.

Claims 47-49 are objected due to their dependency on claim 46

Claims 55-57 are objected due to their dependency on claim 54

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 571-272-2274. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL

MICHAEL NGHIEM
PRIMARY EXAMINER